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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,049	03/24/2005	Ronald Kakoschke	10808/227	1781
7590 Brinks Hofer Gilson & Lione P O Box 10395 Chicago, IL 60610				
EXAMINER				
SALERNO, SARAH KATE				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/529,049

Applicant(s)

KAKOSCHKE, RONALD

Examiner

SARAH K. SALERNO

Art Unit

2814

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 February 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) 10-14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 15-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/26/08 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-2, 4-7 and 15-16 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Sekigawa et al. (US PGPub 2002/0130354 of record) in views of Mistry et al. (US Patent 5,821,575 of record).

Claim 1: Sekigawa teaches an integrated field-effect transistor, having a substrate region surrounded by two terminal regions (10, 11), one terminal region being a source region and the other terminal region being a drain region, the source region being arranged at a first side of the substrate region and the drain region being

arranged at a second side of the substrate region, the first and second sides being opposite sides of the substrate region;

by two electrically insulating layers (71, 72), which are arranged at a third and fourth side of the substrate region, the third and fourth sides being mutually opposite sides of the substrate region (9) and the insulating layers being adjoined by control regions (81,82), the first and second sides being narrower than the third and fourth sides [0032];

by two electrically insulating regions (71,72), the insulating regions being arranged at mutually opposite sides of the substrate region, (FIG. 2-3; [0055-0074]).

Sekigawa does not teach a substrate region surrounded by an electrically conductive connecting region or a part of an electrically conductive connecting region which produces an electrically conductive connection between one of the terminal regions and the substrate region, the connecting region comprising a metal-semiconductor compound, and part of a covering area of the substrate region being covered by the connecting region, such that the connecting region extends across the first side of the substrate region to the source region, the part of the covering area of the substrate region covering the substrate region between the insulating layers and between the control regions. Mistry teaches a substrate region surrounded by an electrically conductive connecting region (35) or a part of an electrically conductive connecting region which produces an electrically conductive connection between one of the terminal regions (28) and the substrate region (26), the connecting region comprising a metal-semiconductor compound, and part of a covering area of the

substrate region being covered by the connecting region, such that the connecting region extends across the first side of the substrate region to the source region, the connecting region covering the substrate region between the insulating layers (44, 22) and between the control regions (45) (FIG. 2-4; Col. 3 lines 20-33, 65-67, Col. 4 lines 1-2) to improve the performance of the device (Col. 1 lines 39-65m Col. 3 lines 1-20). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device to have modified the device taught by Sekigawa to have the body contact region connecting a terminal region and the substrate region to improve the performance of the device as taught by Mistry (FIG. 2-4; Col. 1 lines 39-65m Col. 3 lines 1-20).

Claim 2: Mistry teaches the conductive connecting region at least one of: a silicide of a metal having a melting point of greater than 1400 degrees Celsius, a refractory metal silicide or a rare earth metal silicide (col. 4 lines 1-2),

Claim 4: Sekigawa teaches wherein at least one of one insulating region is part of an insulating layer which carries a multiplicity of field-effect transistors, the insulating layer comprises silicon dioxide, and the other insulating region is part of an insulating layer, which insulates a multiplicity of substrate regions [0059].

Claim 5: Mistry teaches wherein the substrate region at least one of: contains monocrystalline semiconductor material; and is doped in accordance with one conduction type and the terminal regions are doped in accordance with another conduction type (Figure 2,2A).

Claim 6: Sekigawa teaches wherein the control regions are electrically conductively connected to one another [0014].

Claim 7: Sekigawa teaches wherein at least one of: the substrate region contains six side areas, the terminal regions are arranged at mutually opposite sides of the substrate region, the control regions are arranged at mutually opposite sides of the substrate region (Fig. 3)

Claim 15: Mistry teaches the substrate region is p-doped (Figure 2,2A).

Claim 16: Mistry teaches the substrate region is n-doped, thereby producing a p-channel enhancement mode transistor (Col. 8 lines 13-16)

Claim 17: Mistry teaches the insulating regions are arranged at a fifth and sixth side of the substrate region, the fifth and sixth side being arranged at mutually opposite sides of the substrate region (FIG. 4).

4. Claims 3 & 8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Sekigawa et al. (US PGPub 2002/0130354 of record) and Mistry et al. (US Patent 5,821,575 of record), as applied to claim 1 above, and further in view of Smith et al. (US Patent 5,683,918 of record).

Regarding claim 3, as described above, Sekigawa and Mistry substantially read on the invention as claimed, except Sekigawa and Mistry do not specify wherein at least one of: the insulating layers for insulating the control regions from the substrate region have an insulation strength of at least fifteen nanometers a distance between the terminal regions is at least 0.3 micrometer, and one terminal region or both terminal

regions have a shallow doping profile gradient which permits a switching voltage having a magnitude of greater than five volts. Smith teaches wherein at least one of: the insulating layers for insulating the control regions from the substrate region have an insulation strength of at least fifteen nanometers a distance between the terminal regions is at least 0.3 micrometer, and one terminal region or both terminal regions have a shallow doping profile gradient which permits a switching voltage having a magnitude of greater than five volts for ESD protection (Col. 1 lines 55-60, Col. 2 lines 55-65, Col. 4 lines 60-67). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Sekigawa and Mistry to have specified one of insulation strength, distance between terminal regions or switching voltage magnitude to provide the proper ESD protection as taught by Smith (Col. 1 lines 55-60, Col. 2 lines 55-65, Col. 4 lines 60-67).

It is also noted that since it has been held when the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. In *re Aller*, 220 F.2d 454, 105 USPQ 223, 235 (CCPA 1955). Applicant can rebut a prima facie case of obviousness based on ranges by showing unexpected results or the criticality of the claimed range. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claim. In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." In *re Woodruff*, 919 F. 2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP 716.02-716.02(g) for a discussion

of criticality and unexpected results. There is nothing in the present application to indicate that the claimed parameters are critical.

Claim 8: Smith teaches a switching voltage having a magnitude of greater than nine volts are able to be switched by the field-effect transistor.

It is also noted that where the claimed and prior art products are identical or substantially identical in structure or composition or are produced by identical or substantially identical processes, claimed properties or functions are presumed to be inherent. In re Best, 195 USPQ 430, 433 (CCPA 1977). It has also been held that products of identical chemical composition cannot have mutually exclusive properties. A chemical composition and its properties are inseparable. Therefore, if the prior arts teach the identical chemical structure the properties applicant discloses and/or claims are necessarily present. In re Spada, 15 USPQ 2d 1655, 1658 (Fed. Cir. 1990). In this case the field-effect transistor taught by Sekigawa and Mistry would inherently have the property of switching voltages having a magnitude of greater than nine volts, because the field effect transistor taught by Sekigawa and Mistry is structurally identical to the device as claimed in claim 1.

5. Claim 9 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Sekigawa et al. (US PGPub 2002/0130354 of record) and Mistry et al. (US Patent 5,821,575 of record), as applied to claim 1 above, and further in view of Fried et al. (US PGPub 2003/0178670 of record).

Regarding claim 9, as described above, Sekigawa and Mistry substantially read on the invention as claimed, except Sekigawa and Mistry do not teach the field-effect transistor being a driving transistor on a word line or a bit line of a memory cell array, the driving transistor applying a control voltage to the word line or to the bit line. Fried teaches the field-effect transistor being a driving transistor on a word line or a bit line of a memory cell array, the driving transistor applying a control voltage to the word line or to the bit line to increase device density [0018, 0050]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Sekigawa and Mistry to be a driving transistor in a memory cell array to increase device density as taught by Fried [0018, 0050].

Response to Arguments

6. Applicant's arguments filed 09/26/08 have been fully considered but they are not persuasive.

Applicant argues that Mistry's does not teach the connecting region covering the substrate region between the insulating layers and between the control regions. Applicant's arguments are not persuasive because figures 2-4 teach the connecting region (35) between the insulating layers (44 and 22) and the control regions (45's).

Applicant argues that Sekigawa and Mistry do not teach the electrically insulating layers and electrically insulating regions as being distinct elements. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., electrically

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insulating layers and electrically insulating regions being distinct elements) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). *Sekigawa and Mistry* teach the electrically insulating layers and electrically insulating regions as described in the above rejection and as required by the claim limitations.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-R 8:00-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wael M Fahmy/
Supervisory Patent Examiner, Art
Unit 2814

/S. K. S./
Examiner, Art Unit 2814